A 0.4-V 170-μW Fully-Integrated LNA for 2.4-GHz RF Receivers

Giovana P. Ceolin and Lucas Compassi-Severo
Computer Architecture and Microelectronics Group - GAMA
Federal University of Pampa, Alegrete Campus, Alegrete, Brazil
Email: {giovanaceolin.aluno, lucassevero}@unipampa.edu.br

***Abstract*—The low energy requirements of the Internet of Things (IoT) applications have increased the demand for low-power RF receivers. As the low noise amplifier (LNA) is one of the main power-hungry parts of an RF receiver, its power optimization is desired for modern IoT devices. Thus, a 170 μW LNA, able to operate at 2.4 GHz when powered with a 0.4 V power supply is proposed in this work. It is based on an inverter-based amplifier with improved gate bias voltage and automatic forward bulk biasing to operated at the moderated channel inversion level. The post-layout simulated results shown a noise figure of 2.8 dB and competitive specification values in comparison to the state-of-the-art low-voltage LNAs.**

I. Introduction

The Internet of Things (IoT) market has grown a lot in recent years, this is motivated by a large number of usage possibilities. The battery and energy harvesting powered IoT devices have a lifetime directly dependent on the energy consumed by the circuits. Thus, power dissipation reduction is a better strategy to improve the device's lifetime. The RF transceiver used to be the most power-hungry block of the IoT devices, the optimization of this block is very attractive to reduce the overall energy consumption [1].

Several strategies have been proposed in the literature to reduce the power dissipation of the IoT wireless communication, such as the relaxation of the hardware requirements by the communication standard and the development of new RF transceivers topologies. The supply voltage lowering has been demonstrated as an interesting strategy to reduce the power dissipation at the receiver side. Two examples of this are the 2.4 GHz Bluetooth low energy (BLE) receivers presented in [2] and [3] that have shown the power dissipation of 330 μW and 382 μW when powered with 0.18 V and 0.55 V, respectively.

In the RF receiver chain, the low noise amplifier (LNA) is one of the main building blocks since the receiver specifications, as sensibility and power dissipation, are mainly related to this. In general, around 50% of the RF receiver power dissipation can be dissipated by the LNA circuit. It occurs due to the large number of design trade-offs related to the power dissipation, involving the specifications of noise figure (NF), gain, linearity, and input matching [1]. Recent LNA topologies have demonstrated the operation at 2.4 GHz with power dissipation lower than 50 μW, keeping the NF value around 5 dB when powered at the ultra-low voltage (ULV) [4].

In this context, the objective of this work is to analyze the state-of-the-art of low-voltage LNA and to propose a new topology based on the works presented in the literature to allow the operation at the voltage of 0.4 V, using low-cost sub-micron CMOS processes.

This paper is organized as follows, section II presents the analysis of the state-of-the-art of low voltage and low power LNAs, section III presents the proposed LNA and its main characteristics, section IV shows the design and post-layout simulated results and section IV concludes this work.

II. Low Voltage and Low-power LNAs

The operation and design of RF circuits using sub-1V supply voltages is very challenging due to the reduced current density of the MOS transistors at that level. The moderated channel inversion level (MI) is the most favorable region for the RF CMOS transistors operation. The current density at MI is lower than the strong inversion but an improved gate-transconductance to drain-current relation (g_m/I_D) can be obtained. In comparison to the weak inversion, the operation at MI results in reduced parasitic capacitance due to the relatively lower transistor sizes. These characteristics are important to improve the figure-of-merits of an LNA [5].

The MI operation is reached when the transistor gate to source voltage (V_{GS}) is around the threshold voltage (V_T) value. Because of that, MI is also called as near-V_T operation. Thus, the use of the Forward Bulk Bias (FBB) is very important to reduce the V_T and, consequently, reduce the DC V_{GS} level needed to be in the MI operation [6]. Additionally, the use of low voltage supplies also limits the maximum number of stacked transistors in an LNA due to the transistor saturation voltage ($V_{DS_{SAT}}$). Since $V_{DS_{SAT}}$ is around 130 mV at near-V_T, the current reuse technique is limited to no more than 2 stacked devices [7] when powered with 0.4 V, the target of this work.

The LNA proposed in [5] is based on a current reuse resistive feedback topology. This design has used the advantage of the MI operation to obtain higher voltage gain with a good figure of merit. DC blocking capacitors are used to disconnect the AC and DC signals and allow the use of common-gate bias on the NMOS transistor. The circuits can present an input impedance of 50 Ω when an input inductor is used to cancel the input impedance imaginary part. The circuit biasing variability is compensated by a digital-analog converter that adjusts the

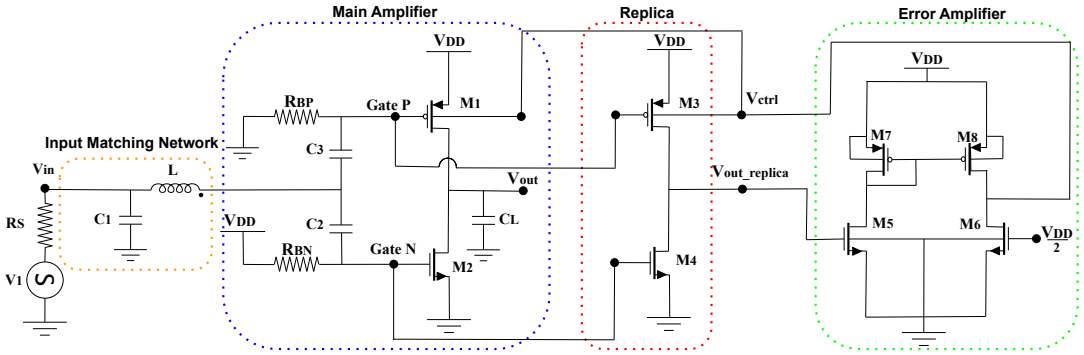

Fig. 1. LNA proposed in this work.

LNA supply voltage. This LNA reaches the power dissipation of 30 μW with operation at 2.4 GHz.

The work of [8], presents single-ended input and balanced outputs. It uses the current reuse technique to decrease the dissipated power, by sharing the DC bias current between NMOS and PMOS transistors. The high-frequency transconductance is improved without any extra energy consumption by using an inductor connected to the gate. Additionally, the use of the gate inductor reduces the effect of parasitic capacitances. In another paper, the same authors have improved the previous LNA by using a g_m boosting technique of shunt feedback cascode topologies to improve the bandwidth without increasing the energy consumption [7]. The FBB is used at the NMOS transistor to reduce the threshold voltage and allow the gate biasing by the out node level. In these implementations, the power dissipation of 410 and 160 μW are obtained, respectively.

In the paper of Ehsan Kargaran [3], a 0.8V LNA is proposed for Wearable Sensor Wireless Networks (W-WSN) applications. To decrease its dissipated power, the LNA was designed using the reuse of the bias current by four stacked transistors and a source resistor. Additionally, the use of a high-quality factor integrated transformer is employed to improve the level of transconductance gain and to reduce power consumption. A simplified version of this topology is presented in [4] where the LNA was able to operate with only 0.18 V of power supply, keeping the same power level of 30 μW.

The LNA proposed by Jian-Yu Hsieh [6], like the previous ULV LNAs, uses FBB biasing techniques to reduce the transistor threshold voltage. The circuit also employs the current reuse technique and multiple gate topology, which makes it possible to eliminate third-order distortion caused by the amplifier's non-linearity and to improve the Input Third-order Intercept Point (IIP3) specification. Another interesting point is the use of a tunable negative feedback capacitor, which makes it possible to obtain the variable gain without additional energy cost, solving possible signal saturation problems.

III. Proposed LNA Topology

The low-voltage LNA circuit shown in Fig. 1 is proposed in this work. It is composed of an integrated input matching network, the main amplifier, a replica circuit, and a pseudo-differential error amplifier. It is based on the topology presented in [5], but we have improved the gate biasing of the PMOS transistor using a DC blocking capacitor to isolate the DC voltage from the output terminal. As a result, the gate DC voltage can be tied to the ground by resistor R_{BP}, increasing the V_{GS} voltage. Similarly, the gate terminal of the NMOS transistor is biased by resistor R_{BN}, tied to V_{DD}.

Furthermore, the DC V_{ctrl} voltage provides an FBB to the PMOS transistor. It is employed to reduce its V_T and also to allow the calibration of the output DC voltage level ($V_{out_{DC}}$) to be equal to $V_{DD}/2$, in order to obtain the best possible gain result in the LNA. The automatic calibration can be performed by using a closed-loop error amplifier that compares $V_{out_{DC}}$ with $V_{DD}/2$ and adjust the V_{ctrl} voltage to make $V_{out_{DC}} \approx V_{DD}/2$. However, the direct connection of the error amplifier to the LNA reduces the operation frequency and gain due to the high capacitive load. To get around this problem, without increasing the power dissipation, a replica bias circuit based in [9] is proposed in this work. The replica transistor has the same bias and size as the main amplifier, but a single multiplicity is used to save power. Thus the closed-loop error amplifier is used to adjust the replica output voltage $V_{DD}/2$. As the replica V_{ctrl} voltage is also applied to the main amplifier, the LNA output voltage is also controlled without any extra load.

The main LNA input impedance (Z_{in}) can be estimated according to (2) that was obtained with the small-signal analysis. Due to the low power dissipation of the proposed LNA, the real part of Z_{in} will be higher than 50 Ω at the operation frequency and its imaginary part will be dominated by the input Miller capacitance due to the feedback parasitic capacitor C_{io}. Thus the C-L network shown in Fig. 1 is used to match Z_{in} with the 50 Ω input impedance.

Using the same small-signal analysis the voltage gain (A_v) and noise figure (N_F) can be estimated according to (3) and (1), respectively.

In these equations, the letters "n" and "p" were used to relate to NMOS and PMOS transistors respectively. The gm is the gate transconductance, gds is the output conductance, γ is the thermal noise parameter, K is the Boltzmann's constant, T is the temperature in Kelvin, s is the Laplace's frequency and the rest are circuit components.

$$N_F = \frac{4.K.T.\left(\frac{\gamma^2(gm_N^2+gm_P^2)}{gds_N^2+gds_P^2+2gds_N.gds_P+\frac{2gds_N+2gds_P}{R_S}+\frac{1}{R_S^2}}+\frac{1}{1+R_S(2gds_N+2gds_P+2R_S.gds_N.gds_P+R_S.gds_N^2+R_S.gds_P^2)}\right)}{R_S(-gm_N-gm_P)} \quad (1)$$

$$Z_{in}(s) = \frac{1}{s(C_{io}+C_i)+\frac{sC_{io}(-sC_{io}+g_{m_n}+g_{m_p})}{sC_{io}+sC_o+g_{ds_n}+g_{ds_p}}} \quad (2)$$

$$A_v(s) = \frac{sC_{io}-g_{m_n}-g_{m_p}}{s(C_{io}+C_o)+g_{ds_n}+g_{ds_p}} \quad (3)$$

IV. Design and Results

The proposed LNA was designed using a 40k$\mathring{A}$ UTM CMOS 180 nm process to operate at the frequency of 2.4 GHz with V_{DD} equal to 0.4 V. The transistors were biased also with V_{GS} equal to 0.4 V to operate near-V_T at the moderate inversion level. The PMOS bulk voltage (V_{ctrl}) is linked to an automatic FBB that allows this voltage to be adjusted to make the output DC voltage equal to $V_{DD}/2$.

The main LNA transistors were sized using an iterative simulation-based process on the Cadence Virtuoso environment. Equations (1) to (3) were used to analyze the specification trade-offs and to lead the iterative process of changing the transistor sizes in order to obtain the smallest power dissipation, higher voltage gain, lower noise figure, and good input matching. It results in the dimensions of L = 300 nm and W = 5 μm to the NMOS and L = 250 nm and W = 4.2 μm to the PMOS transistor, both with 15 multipliers. The transistors used in the replica have the same sizes as the main LNA transistors but using only one multiplier. The error amplifier was designed with a very low current in order to save power, and also to improve the loop stability. Additionally, long channel transistors were employed in the error amplifier to reduce its input offset.

The bias resistors (R_{BP} and R_{BN}) are equal to 100 kΩ to reduce its effect at the input and the DC block capacitor C_2 and C_3 are designed using 8 pF MiM capacitor to present low reactance at 2.4 GHz. The impedance matching was performed with post-layout simulations performed in Cadence's Virtuoso software, where the parasitics were extracted from the layout to obtain a more accurate result. Then, through the Smith chart analyses, the capacitor, and inductor designed to be equal to 0.525 pF and 12.313 nH, respectively.

Fig. 2 shows the layout of the LNA proposed in this work. The complete circuit occupies an area of 19.51 cm^2. Additionally to the previous circuits, an output buffer was used at the LNA output to allow the circuits characterization after the fabrication.

The LNA power dissipation reaches the value of 169.81 μW when powered with 0.4 V. The automatic bias control circuits dissipate about 11.5μ W, less than 7 % of the total dissipated power. Fig. 3 shows the post-layout simulation frequency response of the voltage gain and noise figure (NF). The voltage gain varies from 11.07 dB to 3.758 dB when the frequency varies from 2 to 3 GHz and it is equal to 10.62 dB at 2.4 GHz. The voltage gain at 2.4 GHz can be improved by reducing the input capacitance of the used output buffer. The Noise Figure (NF) is equal to 2.786 dB at the frequency of 2.4 GHz. The input third-order intercept point (IIP_3) is equal to -8.117 dBm, as can be seen in Fig 4.

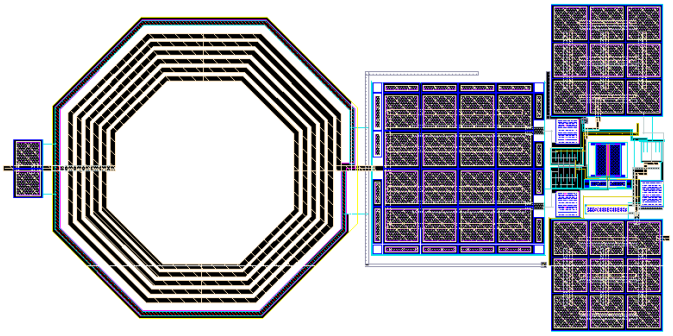

Fig. 2. Layout of the LNA circuit.

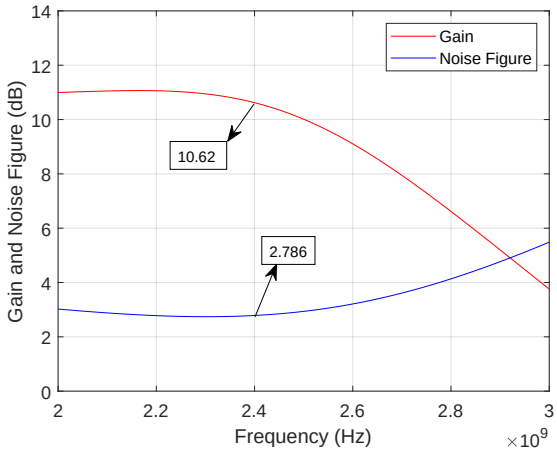

Fig. 3. Frequency response of the voltage gain and noise figure. Gain is equal to 10.62 dB at 2.4 GHz and noise figure is equal to 2.786 dB at 2.4 GHz.

The input matching was analyzed by using the S11 parameter. Fig. 5 shows the simulation of $|S_{11}|$ from 2 to 3 GHz that results in -25.63 dB at 2.4 GHz, showing a good input matching. If the level of $|S_{11}|$ < -10 dB is considered, the designed LNA can reach the bandwidth of 350 MHz, operating from 2.22 GHz to 2.57 GHz.

Table I shows the results obtained with the proposed LNA and a comparison with the state-of-the-art low voltage and low

TABLE I
COMPARISON WITH SOME STATE-OF-THE-ARTS LOW-VOLTAGE LOW-ENERGY LNAS

Specifications	RFIC'11 [5]	ISCAS'13 [8]	JSSC'16 [7]	ISCAS'17 [10]	TCAS-I'18 [4]	TCAS-II'20 [6]	**This Work**	Unit
Voltage	0.4	0.4	0.4	0.8	0.18	0.6	**0.4**	V
Power	60	410	160	30	30	600	**170**	μW
NF	5.3	4.5 $\leftrightarrow$ 5.3	4.5	3.3	5.2	4	**2.786**	dB
Gain	13.1	15	13	14.2	14	4 $\leftrightarrow$ 10	**10.62**	dB
Frequency	2.4	3.2 $\leftrightarrow$ 10	0.6 $\leftrightarrow$ 3.1	2.4	2.4	2.8	**2.4**	GHz
IIP3	-12.2	-2 $\leftrightarrow$ -7	-10	-13.2	-8.6	0	**-8.117**	dBm
Technology	130	90	130	40	40	180	**180**	nm
Means./Sim.	Simulated	Measured	Measured	Simulated	Simulated	Measured	Simulated**	-

* ULV Design, ** Post-Layout

power LNAs, analyzed in section II. It is possible to see that the NF of our work is the lowest value comparing to the other papers, even presenting reduced power dissipation. The rest of the specifications are in the average range of the other papers.

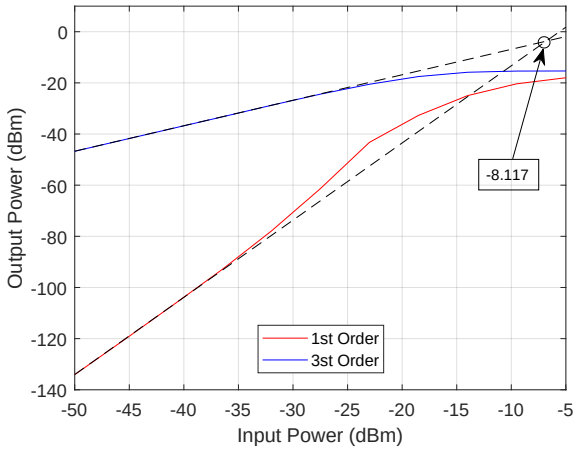

Fig. 4. Output vs input power to obtain the third-order intercept point. The IIP3 is equal -8.117 dBm at 2.4 GHz.

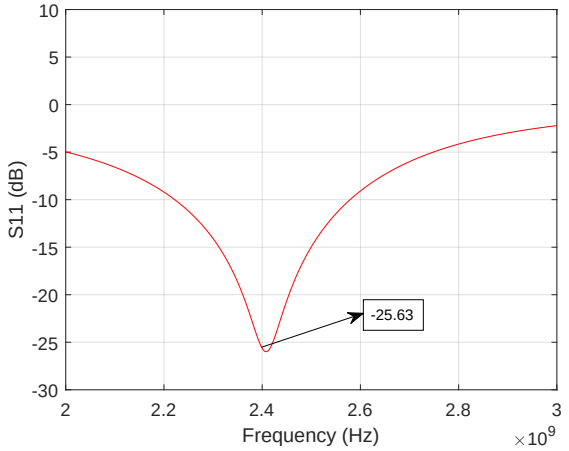

Fig. 5. Frequency response of the S parameters. $|S_{11}|$ is equal to -25.63 dB at 2.4 GHz.

V. CONCLUSION

A 0.4 V low power LNA is presented in this paper to operate at a frequency of 2.4 GHz. The circuit is based on the use of a CMOS feedback amplifier with improved biasing. The results show better performance in terms of noise figure and competitive specification values of gain, IIP3, and power dissipation, with good input matching, compared to the latest generation works.

The circuit is currently being manufactured, in future works, it is intended to measure and compare the simulated results with the measured ones.

ACKNOWLEDGMENT

The authors would like to thank the FAPERGS (Project 19-2551-0001315-9 and PROBITI) for supporting this work and the IEEE EDS for supporting the IC fabrication.

REFERENCES

[1] RAZAVI, Behzad; BEHZAD, Razavi. RF microelectronics. New York: Prentice Hall, 2012.

[2] H. Yi, W. Yu, P. Mak, J. Yin and R. P. Martins, "A 0.18-V 382-μW Bluetooth Low-Energy Receiver Front-End With 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS," IEEE Journal of Solid-State Circuits, vol. 53, no. 6, pp. 1618-1627, 2018.

[3] E. Kargaran, C. Bryant, D. Manstretta, J. Strange and R. Castello, "A Sub-0.6V, 330 µW, 0.15 mm2 Receiver Front-End for Bluetooth Low Energy (BLE) in 22 nm FD-SOI with Zero External Components," 2019 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2019.

[4] E. Kargaran, D. Manstretta and R. Castello, "Design and Analysis of 2.4 GHz 30 μW CMOS LNAs for Wearable WSN Applications," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 3, pp. 891-903, 2018.

[5] T. Taris, J. Begueret and Y. Deval, "A 60 μW LNA for 2.4 GHz wireless sensors network applications," 2011 IEEE Radio Frequency Integrated Circuits Symposium, Baltimore, MD, 2011, pp. 1-4.

[6] J. Hsieh and K. Lin, "A 0.6-V Low-Power Variable-Gain LNA in 0.18-μm CMOS Technology," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, pp. 23-26, Jan. 2020.

[7] M. Parvizi, K. Allidina and M. N. El-Gamal, "Short Channel Output Conductance Enhancement Through Forward Body Biasing to Realize a 0.5 V 250 μA 0.6–4.2 GHz Current-Reuse CMOS LNA," in IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 574-586, March 2016.

[8] M. Parvizi, K. Allidina, F. Nabki and M. El-Gamal, "A 0.4 V ultra low-power UWB CMOS LNA employing noise cancellation," 2013 IEEE International Symposium on Circuits and Systems (ISCAS), Beijing, 2013, pp. 2369-2372.

[9] Compassi-Severo, Lucas and Van Noije, Wilhelmus "A 0.4-V 10.9-μW/Pole Third-Order Complex BPF for Low Energy RF Receivers," in IEEE Transactions on Circuits and Systems I: Regular Papers, 2019.

[10] E. Kargaran, D. Manstretta and R. Castello, "A 30 μW, 3.3 dB NF CMOS LNA for wearable WSN applications," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, 2017, pp. 1-4.